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(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masahiro Matsuo et al.

Application No.: filed concurrently herewith

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Examiner: Not Yet Known

For: METHOD AND APPARATUS FOR POWER SUPPLY CAPABLE OF EFFECTIVELY REDUCING POWER CONSUMPTION

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, DC 20231

Dear Sir:

Please amend the application as follows:

IN THE SPECIFICATION:

Please replace paragraph 0001 with the following:

This patent specification relates to a power supply method and apparatus, and more particularly to a power supply method and apparatus that effectively reduces power consumption.

Please replace paragraph 0003 with the following:

Fig. 1 shows an exemplary circuit of a background power supply apparatus using a voltage

regulator 100. In the voltage regulator 100 of Fig. 1, a P-channel-type MOS (metal oxide semiconductor) transistor 102 (hereinafter referred to as a P-MOS transistor 102) and resisters 103 and 104 are connected in series between a power source terminal applied with a power source voltage VDD by a direct current 101 (e.g., a battery including a secondary battery) and ground. The resisters 103 and 104 divide a voltage Vout which is compared by a voltage comparator 106 with a predetermined reference voltage Vref generated by a reference voltage generator 105. Based on a comparison result, an operation of the P-MOS transistor 102 is controlled so that the voltage Vout is held at a desired value. In Fig. 1, a CPU 107 is an exemplary system that requires power from the voltage regulator 100.

Please replace paragraph 0004 with the following:

However, the above-described voltage regulator has a drawback that the P-MOS transistor 101 consumes a great amount of electric power for a reduction of the power source voltage VDD to the voltage Vout. More specifically, when the CPU 107 consumes a current of 100 mA, for example, and a voltage regulator 100 reduces the power source voltage VDD from 3.6 volts, for example, to 2 volts, for example, the P-MOS transistor 101 consumes the power of 0.16 W. That is, the voltage regulator consumes a difference of the battery voltage and the CPU's operational voltage. Such voltage regulator is undesirable for a system aiming a low power consumption since the CPU's operational voltage has been lowered in the recent years.

Please replace paragraph 0005 with the following:

Accordingly, as shown in Fig. 2, a DC-to-DC converter is used in place of the voltage regulator as a power supply in a system (e.g., the CPU 107) using a battery. In Fig. 2, a DC-to-DC converter 110 reduces the power source voltage VDD to a predetermined voltage Vout and supplies the voltage Vout to the CPU 107.

Please replace paragraph 0006 with the following:

In general, a system using a battery as a source of power is provided with a sleep function for temporarily stopping the operations of the system to reduce an electrical power consumption on an as needed basis. In the case of the power supply apparatus of Fig. 2, it is attempted to reduce the power consumption by changing the output terminal of the DC-to-DC converter 110 to the CPU 107 in the sleep mode from a ground level to a high impedance level. This is because the DC-to-DC converter 110 is used as an apparatus that directly controls the power source required by the system (e.g., the CPU 107).

Please replace paragraph 0008 with the following:

This patent specification describes a novel power supply apparatus. In one example, this novel power supply apparatus includes a DC-to-DC converter and a voltage regulator. The DC-to-DC converter is arranged and configured to perform a voltage conversion for converting a voltage of a power source supplied from a direct current power source to a first predetermined voltage. The first predetermined voltage is lower than the voltage of

the power source. The voltage regulator is arranged and configured to carrying out a voltage regulation for regulating the first predetermined voltage of the power source to at least a second predetermined voltage. The second predetermined voltage is lower than the first predetermined voltage.

Please replace paragraph 0009 with the following:

The DC-to-DC converter may be turned into a non-active state to stop the voltage conversion and straight passes the voltage of the power source when an operation mode is changed to a sleep mode.

Please replace paragraph 0010 with the following:

The DC-to-DC converter may include a switching circuit, a smoothing circuit, and a controller. The switching circuit is arranged and configured to perform a switching operation for switching the power source and to output a pulsating current voltage. The smoothing circuit is arranged and configured to smooth the pulsating current voltage output by the switching circuit and to output a smoothed voltage to the voltage regulator. The controller is arranged and configured to detect the smoothed voltage output from the smoothing circuit and to control the switching circuit to change a performance of the switching operation in response to a detection result of the smoothed voltage so that the smoothed voltage output by the smoothing circuit is substantially equal to the first predetermined voltage. The controller is turned into a non-active state to cause the switching circuit to stop the switching operation so as to pass the voltage of the power

source through the switching circuit and to output the voltage of the power source to the smoothing circuit when the operation mode is changed to the sleep mode.

Please replace paragraph 0011 with the following:

The DC-to-DC converter may output the voltage of the power source without performing the voltage conversion when the operation mode is changed to the sleep mode.

Please replace paragraph 0012 with the following:

The converter may include a switching circuit, a smoothing circuit, and a controller. The switching circuit is arranged and configured to perform a switching operation for switching the power source and outputting a pulsating current voltage. The smoothing circuit is arranged and configured to smooth the pulsating current voltage output from the switching circuit and to output a smoothed voltage to the voltage regulator. The controller is arranged and configured to detect the smoothed voltage output from the smoothing circuit and to control the switching circuit to change a performance of the switching operation in response to a detection result of the smoothed voltage so that the smoothed voltage output from the smoothing circuit is substantially equal to the first predetermined voltage. The controller causes the switching circuit to stop the switching operation so as to pass the voltage of the power source through the switching circuit and to output the voltage of the power source to the smoothing circuit when the operation mode is changed to the sleep mode.

Please replace paragraph 0019 with the following:

The controller may control the switching circuit to straight output the voltage of the power source to the smoothing circuit when the current detected is smaller than a predetermined value and to reduce the current output therefrom to a value smaller than the predetermined value in a predetermined manner when the current is greater than the predetermined value.

Please replace paragraph 0022 with the following:

This patent specification further describes a novel method of power supply. In one example, this novel method includes the steps of performing and regulating. The performing step performs a DC-to-DC conversion with a DC-to-DC converter to achieve a voltage conversion for converting a voltage of a power source supplied from a direct current power source to a first predetermined voltage. The first predetermined voltage is lower than the voltage of the power source. The regulating step regulates the first predetermined voltage of the power source to at least a second predetermined voltage. The second predetermined voltage is lower than the first predetermined voltage.

Please replace paragraph 0023 with the following:

The performing step may turn the DC-to-DC converter into a non-active state to stop the DC-to-DC conversion and straight passes the voltage of the power source through the DC-to-DC converter to the voltage regulator when an operation mode is changed to a sleep mode.

Please replace paragraph 0024 with the following:

The performing step may include the steps of executing, smoothing, detecting, changing, and stopping. The executing step executes a switching operation for switching the power source to output a pulsating current voltage. The smoothing step smoothes the pulsating current voltage output by the switching circuit to output a smoothed voltage to the voltage regulator. The detecting step detects the smoothed voltage output in the smoothing step. The changing step changes a performance of the switching operation in response to a detection result of the smoothed voltage so that the smoothed voltage output in the smoothing step is substantially equal to the first predetermined voltage. The stopping step stops the switching operation when the operation mode is changed to the sleep mode so as to apply the voltage of the power source to the smoothing circuit.

Please replace paragraph 0025 with the following:

The DC-to-DC converter may output the voltage of the power source without performing the voltage conversion when the operation mode is changed to the sleep mode.

Please replace paragraph 0026 with the following:

The performing step may include the steps of executing, smoothing, detecting, changing, and stopping. The executing step executes a switching operation for switching the power source to output a pulsating current voltage. The smoothing step smoothes the pulsating current voltage output in the switching step to output a smoothed voltage to the voltage regulator. The detecting step detects the smoothed voltage output in the smoothing step.

The changing step changes a performance of the switching operation in response to a detection result of the smoothed voltage so that the smoothed voltage output in the smoothing step is substantially equal to the first predetermined voltage. The stopping step stops the switching operation when the operation mode is changed to the sleep mode so as to apply the voltage of the power source to the smoothing circuit.

Please replace paragraph 0033 with the following:

The instructing step may instruct the switching step to straight output the voltage of the power source to the smoothing step when the current detected is smaller than a predetermined value and to reduce the current output in the switching step to a value smaller than the predetermined value in a predetermined manner when the current is greater than the predetermined value.

Please replace paragraph 0045 with the following:

Fig. 9 is a time chart for showing an example of a current Ia flowing through an N-MOS transistor of an undershooting preventive circuit included in the DC-to-DC converter of Fig. 7;

Please replace paragraph 0054 with the following:

As shown in Fig. 3, in the power supply apparatus 1, the DC-to-DC converter 2 is connected between the power supply line from the current power source 10 and ground. The voltage regulator 3 is connected between the output terminal of the DC-to-DC

converter 2 and ground. The output terminal of the voltage regulator 3 is connected to a power supply terminal of a CPU (central processing unit) 11. The CPU 11 is shown as an exemplary device requiring a power supply. Other devices such as a DSP (digital signal processor), memories, and so on which form, together with the CPU 11, a system apparatus also require a power supply.

Please replace paragraph 0055 with the following:

The voltage regulator 3 includes a P-channel-type MOS (metal oxide semiconductor) transistor 21 (hereinafter referred to as a P-MOS transistor 21), resisters 22 and 23, a reference voltage generator 24, and a voltage comparator 25. The P-MOS transistor 21 and the resisters 22 and 23 are connected in series between the output terminal of the DC-to-DC converter 2 and ground, and the voltage regulator 3 has an output terminal drawn from a line connecting the P-MOS transistor 21 to the resister 22. The voltage comparator 25 has an input terminal connected to a line placed between the resisters 22 and 23 and another input terminal to receive a reference voltage Vref output from the reference voltage generator 24. The voltage comparator 25 has an output terminal connected to a gate of the P-MOS transistor 21.

Please replace paragraph 0056 with the following:

The resisters 22 and 23 divide the voltage Vb, and the voltage comparator 25 compares the voltage divided by the resisters 22 and 23 to the reference voltage Vref output from the reference voltage generator 24. When the divided voltage is equal to or greater than the

reference voltage Vref, the voltage comparator 25 controls the operation of the P-MOS transistor 21 so that the current flowing through the P-MOS transistor 21 is reduced. On the other hands, when the divided voltage is smaller than the reference voltage Vref, the voltage comparator 25 controls the P-MOS transistor 21 to increase the flowing current.

Please replace paragraph 0058 with the following:

The voltage regulator 3 reduces the voltage Va applied as a power source by the DC-to-DC converter 2 to obtain the voltage Vb and supplies the voltage Vb to the CPU 11 as a power source. In this way, the power supply apparatus 1 reduces the power source voltage VDD supplied by the direct current power source 10 to the voltage Va with the DC-to-DC converter 2, further reduces the voltage Va to the voltage Vb with the voltage regulator 3, and supplies the voltage Vb as a power source to the CPU 11. With this configuration, it is possible to minimize a value of voltage that the voltage regulator 3 bears to reduce as a load. When the power source voltage VDD is 3.6 volts, for example, the voltage Va output by the DC-to-DC converter 2 may be set to 2.0 volts, for example, and the voltage Vb output by the voltage regulator 3 may be set to 1.8 volts, for example. Thus, the power consumption of the voltage regulator 3 can be reduced.

Please replace paragraph 0059 with the following:

In the sleep mode, that is, during the time the DC-to-DC converter 2 receives the sleep signal SLP from the CPU 11, the DC-to-DC converter 2 is put into an inactive status to stop its operation. When stopping the operation, the DC-to-DC converter 2 outputs the

power source voltage VDD supplied by the direct current power source 10 straight as the voltage Va without performing the voltage reduction. Accordingly, the power source voltage VDD is applied as a power source to the voltage regulator 3. At this time, however, the CPU 11 operates in the sleep mode and consumes almost no electric power. Therefore, the voltage regulator 3 consumes almost no electric power.

Please replace paragraph 0060 with the following:

On the other hands, the CPU 11 may perform its operation at intervals of a relatively short time period (e.g., 1 second) during the sleep mode. In such an operation mode at intervals, the voltage regulator 3 reduces the power source voltage VDD applied thereto through the DC-to-DC converter 2 to the voltage Vb, thereby obtaining a power source required for the CPU 11 to operate. At this time, the electric power consumed by the CPU 11 is relatively small and therefore the P-MOS transistor 21 of the voltage regulator 3 consumes a relatively small amount of electric power.

Please replace paragraph 0063 with the following:

The smoothing circuit 32 includes a smoothing choke coil 45, a smoothing capacitor 46, and a flywheel diode 47. The smoothing choke coil 45 and the smoothing capacitor 46 form a choke input type smoothing circuit that smoothes the pulsating current voltage input from the P-MOS transistor 41 and outputs a resultant voltage. The flywheel diode 47 has a cathode connected to an input terminal of the smoothing choke coil 45 and an anode connected to ground.

Please replace paragraph 0068 with the following:

Fig. 5 shows a DC-to-DC converter 202 which can be used as an alternative to the DC-to-DC converter 2. The DC-to-DC converter 202 of Fig. 5 is similar to the DC-to-DC converter 2 of Fig. 4, except for a smoothing circuit 232 and a controller 233. The smoothing circuit 232 includes a high active N-channel-type MOS (metal oxide semiconductor) transistor 51 (hereinafter referred to as a N-MOS transistor 51) in place of the flywheel diode 47 of the smoothing circuit 32. The controller 233 of Fig. 5 is similar to the controller 33 of Fig. 4, except for generation of control signals S1 and S2. In the DC-to-DC converter 202, the N-MOS transistor 51 is connected between the drain of the P-MOS transistor 41 and ground, as shown in Fig. 5, so that the P-MOS transistor 41 and the N-MOS transistor 51 are controlled by the controller 233 with the control signals S1 and S2.

Please replace paragraph 0069 with the following:

A time chart of Fig. 6 shows a relationship between the control signals S2 and S2. A shown in Fig. 6, the sleep signal SLP output by the CPU 11 is held at a low level during the normal operation mode and at a high level during the sleep mode. During the normal operation mode, the controller 233 generates the control signals S1 and S2 which rise and fall differently from each other and sends them to the P-MOS transistor 41 and the N-MOS transistor 51, respectively. Thereby, the P-MOS transistor 41 and the N-MOS transistor 51 are controlled so as not to be turned on at the same time. This N-MOS

transistor 51 can be integrated with the switching circuit 31, the controller 233, and the voltage regulator 3 into a single IC chip.

Please replace paragraph 0070 with the following:

In this way, the power supply apparatus 1 generates and supplies the stable predetermined voltage Vb to the CPU 11 during the time the CPU 11 operates in the normal operation mode by efficiently reducing the power source voltage VDD to the voltage Va with the DC-to-DC converter 202 and finally regulating the voltage Va with the voltage regulator 3 to obtain the voltage Vb. Thereby, the power supply apparatus 1 can achieve a relatively low power consumption of the voltage regulator 3 in the normal operation mode. Also, during the sleep mode, the power supply apparatus 1 causes the DC-to-DC converter 202 to turn into an inactive state to reduce the power consumption, and generates the predetermined stable Vb by reducing the power source voltage VDD to the voltage Vb directly with the voltage regulator 3. That is, since devices including the CPU, the DSP, memories, etc. are turned into the sleep mode and do not need the power source, the voltage Vb is not used by the devices and no power is consumed. When the CPU 11, for example, operates at intervals of a predetermined time period (e.g., one second) in the sleep mode, the CPU 11 can operate with the stable voltage Vb supplied.

Please replace paragraph 0074 with the following:

That is, at the end of the transition time, the voltage regulator 3 starts its operation under the condition that the voltage Vo is maintained at a voltage level around the power source

voltage VDD. This causes the DC-to-DC converter 302 to fall to a state of being loaded by the voltage regulator 3. In this case, when a load current Io (e.g., 200 mA) flows from the smoothing circuit 32, the voltage Vo may be dropped so rapidly as to produce an undershooting waveform W1, as shown in Fig. 8. As a result, the voltage Vo is momentarily reduced to a value considerably smaller than the predetermined voltage Va.

Please replace paragraph 0075 with the following:

On the other hands, the voltage Vo may rise so rapidly as to produce an overshooting waveform W2, as shown in Fig. 8, when the P-MOS transistor 41 is turned on immediately after the mode is changed from the normal operation mode to the sleep mode in order to cause the power source voltage VDD to pass through the P-MOS transistor 41. In this case, the voltage Vo may produce an overshooting waveform W2, as shown in Fig. 8 and is momentarily risen over a value considerably greater than the power source voltage VDD.

Please replace paragraph 0077 with the following:

The duty control circuit 61 includes a voltage detection circuit 71 and a duty controller 72. The voltage detection circuit 71 detects the voltage Vo, and the duty controller 72 controls a duty cycle of a pulse signal input to the gate of the P-MOS transistor 41 in response to the voltage Vo detected by the voltage detection circuit 71. The voltage detection circuit 71 includes an operational amplifier 73, a voltage dividing circuit 74, a Vr1 generator 75. The voltage dividing circuit 74 divides the voltage Vo, and includes resisters 76 and 77 and an N-channel-type MOS (metal oxide semiconductor) transistor 78 (hereinafter referred to

as an N-MOS transistor 78). The Vr1 generator 75 generates a reference voltage Vr1. The resisters 76 and 77 are connected in series between the line of the voltage Vo and ground. The N-MOS transistor 78 has a gate that receives an inverse sleep signal SLPB (not shown) generated by the inverse of the sleep signal SLP.

Please replace paragraph 0080 with the following:

The undershoot preventive circuit 62 includes an N-channel-type MOS (metal oxide semiconductor) transistor 81 (hereinafter referred to as an N-MOS transistor 81), an operations amplifier 83, and a current control circuit 83. The N-MOS transistor 81 operates as a load to consume a current Ia flowing from the output terminal of the smoothing circuit 32 to ground. The operational amplifier 82 operates as a voltage comparator for comparing the divided voltage Vd output from the voltage dividing circuit 74 to the reference voltage Vr1 output from the Vr1 generator 75, and outputs a binary signal in response to the comparison result. The undershoot preventive circuit 62 further includes a current control circuit 83. The current control circuit 83 controls the operation of the N-MOS transistor 81 in accordance with the signal output from the operational amplifier 82 so as to control the current Ia flowing from the output terminal of the smoothing circuit 32. The operational amplifier 82, the voltage dividing circuit 74, and the Vr1 generator 75 together form a voltage determination circuit.

Please replace paragraph 0081 with the following:

In the undershoot preventive circuit 62, when the mode is changed from the normal operation mode to the sleep mode, the sleep signal SLP in a high state is output from the CPU 11. Accordingly, the operational amplifier 82 and the current control circuit 83 are caused to stop the respective operations and, at the same time, the gate of the N-MOS transistor 81 is turned off and is out of conduction. Since the P-MOS transistor 41 is in an on state and is conducting, the voltage Vo is held at a level around the power source voltage VDD.

Please replace paragraph 0083 with the following:

When the low signal is input from the operational amplifier 82 to the current control circuit 83, the current control circuit 83 raises a gate voltage Vg of the N-MOS transistor 81. As a result, the N-MOS transistor 81 generate the current Ia in response to the gate voltage Vg input, as shown in Fig. 9. The voltage Vd is gradually reduced from the level of the power source voltage VDD to the predetermined voltage Va. During this reduction of the voltage Vd, the operational amplifier 82 changes the output from the low voltage to a high level voltage when the divided voltage Vd is reduced to a level smaller than the reference voltage Vr1.

Please replace paragraph 0084 with the following:

When the operational amplifier 82 outputs a high signal to the current control circuit 83, the current control circuit 83 controls the gate voltage Vg of the N-MOS transistor 81 in a way as shown in Fig. 10. That is, the gate voltage Vg is linearly raised during a

predetermined time t1 and is continuously raised during a predetermined time t2. Further, the gate voltage Vg is held at a level of the power source voltage VDD during a predetermined time t3 and is reduced from the level of the voltage Vg to ground level during a predetermined time t4. During these operations, the current Ia flowing through the N-MOS transistor 81 is changed in a way as shown in Fig. 9. The current during the predetermined time t3 is a saturated current. Also, during these operations, the voltage level of the gate voltage Vg is changed in a way as shown in Fig. 10. The gate voltage Vg is continuously raised in the predetermined time t2 at the same voltage raising pace as in a predetermined time t1 after the predetermined time t1, as shown in Fig. 10. This is because the duty control circuit 72 takes a certain delay time before starting the control of the operation of the P-MOS transistor 41 after the voltage level of the voltage Vo is changed to the predetermined voltage Va.

Please replace paragraph 0086 with the following:

The current control circuit 83 is previously provided with various kinds of settings associated with the gate voltage of the N-MOS transistor 81 so that the voltage regulator 3 starts its operation and the load current IOU flows from the smoothing circuit 32 through the voltage regulator 3 during the time the current control circuit 83 reduces the gate voltage of the N-MOS transistor 81 to ground level. More specifically, the above-mentioned various kinds of settings includes the voltage raising pace of the gate voltage Vg of the N-MOS transistor 81, the predetermined times t2 and t3 in which the gate voltage

Vg is held at the level of the power source voltage VDD, and the pace of reducing the gate voltage Vg from the level of the power source voltage VDD to the ground level.

Please replace paragraph 0089 with the following:

When the above-described operations are performed, the voltage Vo is changed in a way as shown in Fig. 12. As a result, the voltage Vo can be prevented from the undershooting during the time the mode is changed from the sleep mode to the normal operation mode and from the overshooting during the time the mode is changed from the normal operation mode to the sleep mode. In addition, the overshoot preventive circuit 63 also prevents an excessive current flowing from the P-MOS transistor 41 in the sleep mode when a short circuit occurs in a load connected to the smoothing circuit 32. With this, the power supply apparatus 1 can prevent an excessive current output from the DC-to-DC converter 2 in the sleep mode.

Please replace paragraph 0100 with the following:

This patent specification is based on Japanese patent applications, No. JPAP2001-038394 filed on February 15, 2001 and No. JPAP2001-189792 filed on June 22, 2001 in the Japanese Patent Office, the entire contents of which are incorporated by reference herein.

IN THE CLAIMS:

Please amend the claims as follows:

1. (amended) A power supply apparatus, comprising:

a DC-to-DC converter for converting a voltage of a power source supplied from a direct current power source to a first predetermined voltage, said first predetermined voltage being lower than said voltage of said source power; and

a voltage regulator for regulating said first predetermined voltage of said source power to at least a second predetermined voltage, said second predetermined voltage being lower than said first predetermined voltage.

2. (amended) The power supply apparatus of Claim 1, wherein said DC-to-DC converter is turned into a non-active state to stop said voltage conversion and passes said voltage of said power source when an operation mode is changed to a sleep mode.

3. (amended) The power supply apparatus of Claim 2, wherein said DC-to-DC converter comprising:

a switching circuit arranged and configured to perform a switching operation for switching said power source and to output a pulsating current voltage;

a smoothing circuit configured to smooth said pulsating current voltage output by said switching circuit and to output a smoothed voltage to said voltage regulator; and

a controller configured to detect said smoothed voltage output from said smoothing circuit and to control said switching circuit to change a performance of said switching operation in response to a detection result of said smoothed voltage so that said smoothed voltage output by said smoothing circuit is substantially equal to said first predetermined voltage,

wherein said controller is turned into a non-active state to cause said switching circuit to stop said switching operation so as to pass said voltage of said power source through said

switching circuit and to output said voltage of said power source to said smoothing circuit when said operation mode is changed to said sleep mode.

4. (amended) The power supply apparatus of Claim 1, wherein said DC-to-DC converter outputs said voltage of said power source without performing said voltage conversion when said operation mode is changed to said sleep mode.

5. (amended) The power supply apparatus of Claim 4, wherein said converter comprising:

a switching circuit for switching said power source and outputting a pulsating current voltage;

a smoothing circuit for smoothing said pulsating current voltage output from said switching circuit and to output a smoothed voltage to said voltage regulator; and

a controller configured to detect said smoothed voltage output from said smoothing circuit and to control said switching circuit to change said switching operation in response to a detection result of said smoothed voltage so that said smoothed voltage output from said smoothing circuit is substantially equal to said first predetermined voltage,

wherein said controller causes said switching circuit to stop said switching operation so as to pass said voltage of said power source through said switching circuit and to output said voltage of said power source to said smoothing circuit when said operation mode is changed to said sleep mode.

6. (amended) The power supply apparatus of Claim 5, wherein said controller connects a load to an output terminal of said smoothing circuit and controls a current flowing

said load so as to reduce said voltage output from said smoothing circuit to said first predetermined voltage when said voltage output from said smoothing circuit is lower than said first predetermined voltage and when said operation mode is changed to a normal operation mode.

7. (amended) The power supply apparatus of Claim 6, wherein said controller comprises:

a transistor which operates as said load;

a comparator for comparing said voltage output from said smoothing circuit with said first predetermined voltage when said operation mode is changed to said normal operation mode and outputs a first comparison result; and

a current control circuit configured to control said transistor to produce a current flowing therethrough in response to said first comparison result of said comparator when said operation mode is changed to said normal operation mode.

8. (amended) The power supply apparatus of Claim 7, wherein said current control circuit controls said transistor to increase said current at a first predetermined pace when said voltage output from said smoothing circuit is determined as greater than said first predetermined voltage based on said first comparison result performed by said comparator.

9. (amended) The power supply apparatus of Claim 7, wherein said current control circuit controls said transistor to continue to increase said current at said first predetermined pace for a first predetermined time period when said voltage output from said smoothing circuit is determined as substantially equal to said first predetermined voltage based on said first

comparison result performed by said comparator, and controls said transistor to produce a saturated current flowing therethrough for a second predetermined time period immediately after said first predetermined time period.

10. (amended) The power supply apparatus of Claim 9, wherein said current control circuit controls said transistor to decrease said current at a second predetermined pace for a third predetermined time period immediately after said second predetermined time period.

11. (amended) The power supply apparatus of Claim 5, wherein said controller detects a current output from said switching circuit and controls said switching circuit to vary said current in response to said detected current when said operation mode is changed to said sleep mode.

12. (amended) The power supply apparatus of Claim 11, wherein said controller controls said switching circuit to straight output said voltage of said power source to said smoothing circuit when said current detected is smaller than a predetermined value and to reduce said current output therefrom to a value smaller than said predetermined value in a predetermined manner when said current is greater than said predetermined value.

13. (amended) The power supply apparatus of Claim 5, wherein said controller performs a second comparison between a reference voltage dropping at a substantially constant pace and said voltage output from said smoothing circuit in response to said detected voltage and, according to a result of said second comparison, controls a duty cycle of said switching operation performed by said switching circuit during a time said voltage output from said

smoothing circuit is reduced to said first predetermined voltage, when said operation mode is changed to said normal operation mode.

14. (amended) The power supply apparatus of Claim 13, wherein said controller performs a third comparison between another predetermined reference voltage and said voltage output from said smoothing circuit in response to said detected voltage and, according to a result of said third comparison, controls a duty cycle of said switching operation performed by said switching circuit when said voltage output from said smoothing circuit is reduced to said first predetermined voltage.

15. (amended) A power supply apparatus, comprising:

converting means for performing a DC-to-DC conversion for converting a voltage of a power source supplied from a direct current power source to a first predetermined voltage, said first predetermined voltage being lower than said voltage of said power source; and

regulating means for carrying out a voltage regulation for regulating said first predetermined voltage of said power source to at least a second predetermined voltage, said second predetermined voltage being lower than said first predetermined voltage.

16. (amended) The power supply apparatus of Claim 15, wherein said converting means is turned into a non-active state to stop said voltage conversion and straight passes said voltage of said power source when an operation mode is changed to a sleep mode.

17. (amended) The power supply apparatus of Claim 16, wherein said DC-to-DC converter comprising:

switching means for switching said power source and outputting a pulsating current voltage;

smoothing means for smoothing said pulsating current voltage output by said switching means and to output a smoothed voltage to said regulating means; and

controlling means for detecting said smoothed voltage output from said smoothing means and to control said switching means to change a performance of said switching operation in response to a detection result of said smoothed voltage so that said smoothed voltage output by said smoothing means is substantially equal to said first predetermined voltage,

wherein said controlling means is turned into a non-active state to cause said switching means to stop said switching operation so as to pass said voltage of said power source through said switching means and to output said voltage of said power source to said smoothing means when said operation mode is changed to said sleep mode.

18. (amended) The power supply apparatus of Claim 15, wherein said converting means outputs said voltage of said power source without performing said voltage conversion when said operation mode is changed to said sleep mode.

19. (amended) The power supply apparatus of Claim 18, wherein said converting means comprising:

switching means for switching said power source and outputting a pulsating current voltage;

smoothing means for smoothing said pulsating current voltage output from said switching means and to output a smoothed voltage to said regulating means; and

controlling means for detecting said smoothed voltage output from said smoothing means and to control said switching means to change a performance of said switching operation in response to a detection result of said smoothed voltage so that said smoothed voltage output from said smoothing means is substantially equal to said first predetermined voltage,

wherein said controlling means causes said switching means to stop said switching operation so as to pass said voltage of said power source through said switching means and to output said voltage of said power source to said smoothing means when said operation mode is changed to said sleep mode.

20. (amended) The power supply apparatus of Claim 19, wherein said controlling means connects a load to an output terminal of said smoothing means and controls a current flowing through said load so as to reduce said voltage output from said smoothing means to said first predetermined voltage when said voltage output from said smoothing means is lower than said first predetermined voltage and when said operation mode is changed to a normal operation mode.

21. (amended) The power supply apparatus of Claim 20, wherein said controlling means comprising:

a transistor which operates as said load;

comparing means for performing a first comparison for comparing said voltage output from said smoothing means with said first predetermined voltage when said operation mode is changed to said normal operation mode and outputs a first comparison result; and

current controlling means controlling said transistor to produce a current flowing therethrough in response to said first comparison result of said comparing means when said operation mode is changed to said normal operation mode.

22. (amended) The power supply apparatus of Claim 21, wherein said current controlling means controls said transistor to increase said current at a first predetermined pace when said voltage output from said smoothing means is determined as greater than said first predetermined voltage based on said first comparison result performed by said comparing means.

23. (amended) The power supply apparatus of Claim 21, wherein said current controlling means controls said transistor to continue to increase said current at said first predetermined pace for a first predetermined time period when said voltage output from said smoothing means is determined as substantially equal to said first predetermined voltage based on said first comparison result performed by said comparing means, and controls said transistor to produce a saturated current flowing therethrough for a second predetermined time period immediately after said first predetermined time period.

24. (amended) The power supply apparatus of Claim 23, wherein said current controlling means controls said transistor to decrease said current at a second predetermined pace for a third predetermined time period immediately after said second predetermined time period.

25. (amended) The power supply apparatus of Claim 19, wherein said controlling means detects a current output from said switching means and controls said switching means to

vary said current in response to said detected current when said operation mode is changed to said sleep mode.

26. (amended) The power supply apparatus of Claim 25, wherein said controlling means controls said switching means to straight output said voltage of said power source to said smoothing means when said current detected is smaller than a predetermined value and to reduce said current output therefrom to a value smaller than said predetermined value in a predetermined manner when said current is greater than said predetermined value.

27. (amended) The power supply apparatus of Claim 19, wherein said controlling means performs a second comparison between a reference voltage dropping at a substantially constant pace and said voltage output from said smoothing means in response to said detected voltage and, according to a result of said second comparison, controls a duty cycle of said switching operation performed by said switching means during a time said voltage output from said smoothing means is reduced to said first predetermined voltage, when said operation mode is changed to said normal operation mode.

28. (amended) The power supply apparatus of Claim 27, wherein said controlling means performs a third comparison between another predetermined reference voltage and said voltage output from said smoothing means in response to said detected voltage and, according to a result of said third comparison, controls a duty cycle of said switching operation performed by said switching means when said voltage output from said smoothing means is reduced to said first predetermined voltage.

29. (amended) A method of power supply, comprising the steps of:

using a DC-to-DC converter to convert a voltage of a power source supplied from a direct current power source to a first predetermined voltage, said first predetermined voltage being lower than said voltage of said power source; and

regulating said first predetermined voltage of said power source to at least a second predetermined voltage, said second predetermined voltage being lower than said first predetermined voltage.

30. (amended) The method of Claim 29, wherein said performing step turns said DC-to-DC converter into a non-active state to stop said DC-to-DC conversion and passes said voltage of said power source straight through said DC-to-DC converter to said voltage regulator when an operation mode is changed to a sleep mode.

31. (amended) The method of Claim 30, wherein said performing step comprising the steps of:

executing a switching operation for switching said power source to output a pulsating current voltage;

smoothing said pulsating current voltage output by said switching circuit to output a smoothed voltage to said voltage regulator;

detecting said smoothed voltage output in said smoothing step;

changing a performance of said switching operation in response to a detection result of said smoothed voltage so that said smoothed voltage output in said smoothing step is substantially equal to said first predetermined voltage; and

stopping said switching operation when said operation mode is changed to said sleep mode so as to apply said voltage of said power source to said smoothing circuit.

32. (amended) The method of Claim 29, wherein said DC-to-DC converter outputs said voltage of said power source without performing said voltage conversion when said operation mode is changed to said sleep mode.

33. (amended) The method of Claim 32, wherein said performing step comprising the steps of:

executing a switching operation for switching said power source to output a pulsating current voltage;

smoothing said pulsating current voltage output in said switching step to output a smoothed voltage to said voltage regulator;

detecting said smoothed voltage output in said smoothing step;

changing a performance of said switching operation in response to a detection result of said smoothed voltage so that said smoothed voltage output in said smoothing step is substantially equal to said first predetermined voltage; and

stopping said switching operation when said operation mode is changed to said sleep mode so as to apply said voltage of said power source to said smoothing circuit.

34. (amended) The method of Claim 32, further comprising steps of:

providing a transistor as a load;

applying said voltage output in said smoothing step to said transistor so that a current flows through said transistor when said voltage output in said smoothing step is lower than said

first predetermined voltage and when said operation mode is changed to a normal operation mode; and

adjusting said current flowing said load so as to reduce said voltage output in said smoothing step to said first predetermined voltage.

35. (amended) The method of Claim 34, wherein said adjusting step comprising the steps of:

performing a first comparison for comparing said voltage output in said smoothing step with said first predetermined voltage when said operation mode is changed to said normal operation mode to output a first comparison result; and

causing said transistor to produce a current flowing therethrough in response to said first comparison result of said comparing step when said operation mode is changed to said normal operation mode.

36. (amended) The method of Claim 35, wherein said causing step causes said transistor to increase said current at a first predetermined pace when said voltage output in said smoothing step is determined as greater than said first predetermined voltage based on said first comparison result performed in said comparing step.

37. (amended) The method of Claim 35, wherein said causing step causes said transistor to continue to increase said current at said first predetermined pace for a first predetermined time period when said voltage output in said smoothing step is determined as substantially equal to said first predetermined voltage based on said first comparison result performed in said comparing step, and causes said transistor to produce a saturated current

flowing therethrough for a second predetermined time period immediately after said first predetermined time period.

38. (amended) The method of Claim 37, wherein said causing step causes said transistor to decrease said current at a second predetermined pace for a third predetermined time period immediately after said second predetermined time period.

39. (amended) The method of Claim 33, further comprising the steps of:

detecting a current output in said switching step when said operation mode is changed to said sleep mode; and

instructing said switching step to change said current in response to said detected current.

40. (amended) The method of Claim 39, wherein said instructing step instructs said switching step to straight output said voltage of said power source to said smoothing step when said current detected is smaller than a predetermined value and to reduce said current output in said switching step to a value smaller than said predetermined value in a predetermined manner when said current is greater than said predetermined value.

41. (amended) The method of Claim 33, further comprising the steps of:

performing a second comparison between a reference voltage dropping at a substantially constant pace and said voltage output in said smoothing step in response to said detected voltage during a time said voltage output in said smoothing step is reduced to said first predetermined voltage; and

determining a duty cycle of said switching operation performed in said switching step according to a result of said second comparison.

42. (amended) The method of Claim 41, further comprising the steps of:

performing a third comparison between another predetermined reference voltage and said voltage output in said smoothing circuit in response to said detected voltage; and

controlling said duty cycle of said switching operation performed in said switching step according to a result of said third comparison when said voltage output in said smoothing step is reduced to said first predetermined voltage.

REMARKS

The proposed amendments contained herein are to address matters of form only. No new matter has been added. Accordingly, the Examiner is requested to enter this preliminary amendment.

Dated: February 15, 2002

Respectfully submitted,

By________________________

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VERSION WITH MARKINGS TO SHOW CHANGES MADE:

IN THE SPECIFICATION:

Please amend paragraph 0001 as follows:

This patent specification relates to a power supply method and apparatus [for power supply], and more particularly to a power supply method and apparatus [for power supply] that effectively [reducing a] reduces power consumption.

Please amend paragraph 0003 as follows:

Fig. 1 shows an exemplary circuit of a background power supply apparatus using a voltage regulator 100. In the voltage regulator 100 of Fig. 1, a P-channel-type MOS (metal oxide semiconductor) transistor 102 (hereinafter referred to as a P-MOS transistor 102) and resisters 103 and 104 are connected in series between a [source power] power source terminal applied with a [source power] power source voltage VDD by a direct current 101 (e.g., a battery including a secondary battery) and [a grounding] ground. The resisters 103 and 104 divide a voltage Vout which is compared by a voltage comparator 106 with a predetermined reference voltage Vref generated by a reference voltage generator 105. Based on a comparison result, an operation of the P-MOS transistor 102 is controlled so that the voltage Vout is held at a desired value. In Fig. 1, a CPU 107 is an exemplary system that requires power from the voltage regulator 100.

Please amend paragraph 0004 as follows:

However, the above-described voltage regulator has a drawback that the P-MOS transistor 101 consumes a great amount of electric power for a reduction of the [source power] power source voltage VDD to the voltage Vout. More specifically, when the CPU 107 consumes a current of 100 mA, for example, and a voltage regulator 100 reduces the [source power] power source voltage VDD from 3.6 volts, for example, to 2 volts, for example, the P-MOS transistor 101 consumes the power of 0.16 W. That is, the voltage regulator consumes a difference of the battery voltage and the CPU's operational voltage. Such voltage regulator is undesirable for a system aiming a low power consumption since the CPU's operational voltage has been lowered in the recent years.

Please amend paragraph 0005 as follows:

Accordingly, as shown in Fig. 2, a DC-to-DC converter is used in place of the voltage regulator as a power supply in a system (e.g., the CPU 107) using a battery. In Fig. 2, a DC-to-DC converter 110 reduces the [source power] power source voltage VDD to a predetermined voltage Vout and supplies the voltage Vout to the CPU 107.

Please amend paragraph 0006 as follows:

In general, a system using a battery as a source of power is provided with a sleep function for temporarily stopping the operations of the system to reduce an electrical power consumption on an as needed basis. In the case of the power supply apparatus of Fig. 2, it

is attempted to reduce the power consumption by changing the output terminal of the DC-to-DC converter 110 to the CPU 107 in the sleep mode from a [a grounding] ground level to a high impedance level. This is because the DC-to-DC converter 110 is used as an apparatus that directly controls the [source power] power source required by the system (e.g., the CPU 107).

Please amend paragraph 0008 as follows:

This patent specification describes a novel power supply apparatus. In one example, this novel power supply apparatus includes a DC-to-DC converter and a voltage regulator. The DC-to-DC converter is arranged and configured to perform a voltage conversion for converting a voltage of a [source power] power source supplied from a direct current [source power] power source to a first predetermined voltage. The first predetermined voltage is lower than the voltage of the [source power] power source. The voltage regulator is arranged and configured to carrying out a voltage regulation for regulating the first predetermined voltage of the [source power] power source to at least a second predetermined voltage. The second predetermined voltage is lower than the first predetermined voltage.

Please amend paragraph 0009 as follows:

The DC-to-DC converter may be turned into a non-active state to stop the voltage conversion and straight passes the voltage of the [source power] power source when an operation mode is changed to a sleep mode.

Please amend paragraph 0010 as follows:

The DC-to-DC converter may include a switching circuit, a smoothing circuit, and a controller. The switching circuit is arranged and configured to perform a switching operation for switching the [source power] power source and to output a pulsating current voltage. The smoothing circuit is arranged and configured to smooth the pulsating current voltage output by the switching circuit and to output a smoothed voltage to the voltage regulator. The controller is arranged and configured to detect the smoothed voltage output from the smoothing circuit and to control the switching circuit to change a performance of the switching operation in response to a detection result of the smoothed voltage so that the smoothed voltage output by the smoothing circuit is substantially equal to the first predetermined voltage. The controller is turned into a non-active state to cause the switching circuit to stop the switching operation so as to pass the voltage of the [source power] power source through the switching circuit and to output the voltage of the [source power] power source to the smoothing circuit when the operation mode is changed to the sleep mode.

Please amend paragraph 0011 as follows:

The DC-to-DC converter may output the voltage of the [source power] power source without performing the voltage conversion when the operation mode is changed to the sleep mode.

Please amend paragraph 0012 as follows:

The converter may include a switching circuit, a smoothing circuit, and a controller. The switching circuit is arranged and configured to perform a switching operation for switching the [source power] power source and outputting a pulsating current voltage. The smoothing circuit is arranged and configured to smooth the pulsating current voltage output from the switching circuit and to output a smoothed voltage to the voltage regulator. The controller is arranged and configured to detect the smoothed voltage output from the smoothing circuit and to control the switching circuit to change a performance of the switching operation in response to a detection result of the smoothed voltage so that the smoothed voltage output from the smoothing circuit is substantially equal to the first predetermined voltage. The controller causes the switching circuit to stop the switching operation so as to pass the voltage of the [source power] power source through the switching circuit and to output the voltage of the [source power] power source to the smoothing circuit when the operation mode is changed to the sleep mode.

Please amend paragraph 0019 as follows:

The controller may control the switching circuit to straight output the voltage of the [source power] power source to the smoothing circuit when the current detected is smaller than a predetermined value and to reduce the current output therefrom to a value smaller than the predetermined value in a predetermined manner when the current is greater than the predetermined value.

Please amend paragraph 0022 as follows:

This patent specification further describes a novel method of power supply. In one example, this novel method includes the steps of performing and regulating. The performing step performs a DC-to-DC conversion with a DC-to-DC converter to achieve a voltage conversion for converting a voltage of a [source power] power source supplied from a direct current [source power] power source to a first predetermined voltage. The first predetermined voltage is lower than the voltage of the [source power] power source. The regulating step regulates the first predetermined voltage of the [source power] power source to at least a second predetermined voltage. The second predetermined voltage is lower than the first predetermined voltage.

Please amend paragraph 0023 as follows:

The performing step may turn the DC-to-DC converter into a non-active state to stop the DC-to-DC conversion and straight passes the voltage of the [source power] power source through the DC-to-DC converter to the voltage regulator when an operation mode is changed to a sleep mode.

Please amend paragraph 0024 as follows:

The performing step may include the steps of executing, smoothing, detecting, changing, and stopping. The executing step executes a switching operation for switching the [source power] power source to output a pulsating current voltage. The smoothing step smoothes the pulsating current voltage output by the switching circuit to output a smoothed voltage

to the voltage regulator. The detecting step detects the smoothed voltage output in the smoothing step. The changing step changes a performance of the switching operation in response to a detection result of the smoothed voltage so that the smoothed voltage output in the smoothing step is substantially equal to the first predetermined voltage. The stopping step stops the switching operation when the operation mode is changed to the sleep mode so as to apply the voltage of the [source power] power source to the smoothing circuit.

Please amend paragraph 0025 as follows:

The DC-to-DC converter may output the voltage of the [source power] power source without performing the voltage conversion when the operation mode is changed to the sleep mode.

Please amend paragraph 0026 as follows:

The performing step may include the steps of executing, smoothing, detecting, changing, and stopping. The executing step executes a switching operation for switching the [source power] power source to output a pulsating current voltage. The smoothing step smoothes the pulsating current voltage output in the switching step to output a smoothed voltage to the voltage regulator. The detecting step detects the smoothed voltage output in the smoothing step. The changing step changes a performance of the switching operation in response to a detection result of the smoothed voltage so that the smoothed voltage output in the smoothing step is substantially equal to the first predetermined voltage. The

stopping step stops the switching operation when the operation mode is changed to the sleep mode so as to apply the voltage of the [source power] power source to the smoothing circuit.

Please amend paragraph 0033 as follows:

The instructing step may instruct the switching step to straight output the voltage of the [source power] power source to the smoothing step when the current detected is smaller than a predetermined value and to reduce the current output in the switching step to a value smaller than the predetermined value in a predetermined manner when the current is greater than the predetermined value.

Please amend paragraph 0045 as follows:

Fig. 9 is a time chart for showing an example of a current [ia] Ia flowing through an N-MOS transistor of an undershooting preventive circuit included in the DC-to-DC converter of Fig. 7;

Please amend paragraph 0054 as follows:

As shown in Fig. 3, in the power supply apparatus 1, the DC-to-DC converter 2 is connected between the power supply line from the current [source power] power source 10 and [the grounding] ground. The voltage regulator 3 is connected between the output terminal of the DC-to-DC converter 2 and [the grounding] ground. The output terminal of the voltage regulator 3 is connected to a power supply terminal of a CPU (central

processing unit) 11. The CPU 11 is shown as an exemplary device requiring a power supply. Other devices such as a DSP (digital signal processor), memories, and so on which form, together with the CPU 11, a system apparatus also require a power supply.

Please amend paragraph 0055 as follows:

The voltage regulator 3 includes a P-channel-type MOS (metal oxide semiconductor) transistor 21 (hereinafter referred to as a P-MOS transistor 21), resisters 22 and 23, a reference voltage generator 24, and a voltage comparator 25. The P-MOS transistor 21 and the resisters 22 and 23 are connected in series between the output terminal of the DC-to-DC converter 2 and [the grounding] ground, and the voltage regulator 3 has an output terminal drawn from a line connecting the P-MOS transistor 21 to the resister 22. The voltage comparator 25 has an input terminal connected to a line placed between the resisters 22 and 23 and another input terminal to receive a reference voltage Vref output from the reference voltage generator 24. The voltage comparator 25 has an output terminal connected to a gate of the P-MOS transistor 21.

Please amend paragraph 0056 as follows:

The resisters 22 and 23 divide the voltage Vb, and the voltage comparator 25 compares the voltage divided by the resisters 22 and 23 to the reference voltage Vref output from the reference voltage generator 24. When the divided voltage is equal to or greater than the reference voltage Vref, the voltage comparator 25 controls the operation of the P-MOS transistor 21 so that [a] the current flowing through the P-MOS transistor 21 is reduced.

On the other hands, when the divided voltage is smaller than the reference voltage Vref, the voltage comparator 25 controls the P-MOS transistor 21 to increase the flowing current.

Please amend paragraph 0058 as follows:

The voltage regulator 3 reduces the voltage Va applied as a [source power] power source by the DC-to-DC converter 2 to obtain the voltage Vb and supplies the voltage Vb to the CPU 11 as a [source power] power source. In this way, the power supply apparatus 1 reduces the [source power] power source voltage VDD supplied by the direct current [source power] power source 10 to the voltage Va with the DC-to-DC converter 2, further reduces the voltage Va to the voltage Vb with the voltage regulator 3, and supplies the voltage Vb as a [source power] power source to the CPU 11. With this configuration, it is possible to minimize a value of voltage that the voltage regulator 3 bears to reduce as a load. When the [source power] power source voltage VDD is 3.6 volts, for example, the voltage Va output by the DC-to-DC converter 2 may be set to 2.0 volts, for example, and the voltage Vb output by the voltage regulator 3 may be set to 1.8 volts, for example. Thus, the power consumption of the voltage regulator 3 can be reduced.

Please amend paragraph 0059 as follows:

In the sleep mode, that is, during the time the DC-to-DC converter 2 receives the sleep signal SLP from the CPU 11, the DC-to-DC converter 2 is put into an inactive status to stop its operation. When stopping the operation, the DC-to-DC converter 2 outputs the

[source power] power source voltage VDD supplied by the direct current [source power] power source 10 straight as the voltage Va without performing the voltage reduction. Accordingly, the [source power] power source voltage VDD is applied as a [source power] power source to the voltage regulator 3. At this time, however, the CPU 11 operates in the sleep mode and consumes almost no electric power. Therefore, the voltage regulator 3 consumes almost no electric power.

Please amend paragraph 0060 as follows:

On the other hands, the CPU 11 may perform its operation at intervals of a relatively short time period (e.g., 1 second) during the sleep mode. In such an operation mode at intervals, the voltage regulator 3 reduces the [source power] power source voltage VDD applied thereto through the DC-to-DC converter 2 to the voltage Vb, thereby obtaining a [source power] power source required for the CPU 11 to operate. At this time, the electric power consumed by the CPU 11 is relatively small and therefore the P-MOS transistor 21 of the voltage regulator 3 consumes a relatively small amount of electric power.

Please amend paragraph 0063 as follows:

The smoothing circuit 32 includes a smoothing choke coil 45, a smoothing capacitor 46, and a flywheel diode 47. The smoothing choke coil 45 and the smoothing capacitor 46 form a choke input type smoothing circuit that smoothes the pulsating current voltage input from the P-MOS transistor 41 and outputs a resultant voltage. The flywheel diode

47 has a cathode connected to an input terminal of the smoothing choke coil 45 and an anode connected to [the grounding] ground.

Please amend paragraph 0068 as follows:

Fig. 5 shows a DC-to-DC converter 202 which can be used as an alternative to the DC-to-DC converter 2. The DC-to-DC converter 202 of Fig. 5 is similar to the DC-to-DC converter 2 of Fig. 4, except for a smoothing circuit 232 and a controller 233. The smoothing circuit 232 includes a high active N-channel-type MOS (metal oxide semiconductor) transistor 51 (hereinafter referred to as a N-MOS transistor 51) in place of the flywheel diode 47 of the smoothing circuit 32. The controller 233 of Fig. 5 is similar to the controller 33 of Fig. 4, except for generation of control signals S1 and S2. In the DC-to-DC converter 202, the N-MOS transistor 51 is connected between the drain of the P-MOS transistor 41 and [the grounding] ground, as shown in Fig. 5, so that the P-MOS transistor 41 and the N-MOS transistor 51 are controlled by the controller 233 with the control signals S1 and S2.

Please amend paragraph 0069 as follows:

A time chart of Fig. 6 shows a relationship between the control signals S2 and S2. A shown in Fig. 6, the sleep signal SLP output by the CPU 11 is held at a low level during the normal operation mode and at a high level during the sleep mode. During the normal operation mode, the controller 233 generates the control signals S1 and S2 which [differently] rise and fall differently from each other and sends them to the P-MOS

transistor 41 and the N-MOS transistor 51, respectively. Thereby, the P-MOS transistor 41 and the N-MOS transistor 51 are controlled so as not to be turned on at the same time. This N-MOS transistor 51 can be integrated with the switching circuit 31, the controller 233, and the voltage regulator 3 into a single IC chip.

Please amend paragraph 0070 as follows:

In this way, the power supply apparatus 1 generates and supplies the stable predetermined voltage Vb to the CPU 11 during the time the CPU 11 operates in the normal operation mode by efficiently reducing the [source power] power source voltage VDD to the voltage Va with the DC-to-DC converter 202 and finally regulating the voltage Va with the voltage regulator 3 to obtain the voltage Vb. Thereby, the power supply apparatus 1 can achieve a relatively low power consumption of the voltage regulator 3 in the normal operation mode. Also, during the sleep mode, the power supply apparatus 1 causes the DC-to-DC converter 202 to turn into an inactive state to reduce the power consumption, and generates the predetermined stable Vb by reducing the [source power] power source voltage VDD to the voltage Vb directly with the voltage regulator 3. That is, since [the] devices including the CPU, the DSP, [the] memories, etc. are turned into the sleep mode and do not need the [source power] power source, the voltage Vb is not used by the devices and no power is consumed. When the CPU 11, for example, operates at intervals of a predetermined time period (e.g., one second) in the sleep mode, the CPU 11 can operate with the stable voltage Vb supplied.

Please amend paragraph 0074 as follows:

That is, at the end of the transition time, the voltage regulator 3 starts its operation under the condition that the voltage Vo is maintained at a voltage level around the power source voltage VDD. This causes the DC-to-DC converter 302 to fall to a state of being loaded by the voltage regulator 3. In this case, when a load current [io] Io (e.g., 200 mA) flows from the smoothing circuit 32, the voltage Vo may be dropped so rapidly as to produce an undershooting waveform W1, as shown in Fig. 8. As a result, the voltage Vo is momentarily reduced to a value considerably smaller than the predetermined voltage Va.

Please amend paragraph 0075 as follows:

On the other hands, the voltage Vo may [be risen] rise so rapidly as to produce an overshooting waveform W2, as shown in Fig. 8, when the P-MOS transistor 41 is turned on immediately after the mode is changed from the normal operation mode to the sleep mode in order to cause the [source power] power source voltage VDD to pass through the P-MOS transistor 41. In this case, the voltage Vo may produce an overshooting waveform W2, as shown in Fig. 8 and is momentarily risen over a value considerably greater than the [source power] power source voltage VDD.

Please amend paragraph 0077 as follows:

The duty control circuit 61 includes a voltage detection circuit 71 and a duty controller 72. The voltage detection circuit 71 detects the voltage Vo, and the duty controller 72 controls a duty cycle of a pulse signal input to the gate of the P-MOS transistor 41 in response to

the voltage Vo detected by the voltage detection circuit 71. The voltage detection circuit 71 includes an operational amplifier 73, a voltage dividing circuit 74, a Vr1 generator 75. The voltage dividing circuit 74 divides the voltage Vo, and includes resisters 76 and 77 and an N-channel-type MOS (metal oxide semiconductor) transistor 78 (hereinafter referred to as an N-MOS transistor 78). The Vr1 generator 75 generates a reference voltage Vr1. The resisters 76 and 77 are connected in series between the line of the voltage Vo and [the grounding] ground. The N-MOS transistor 78 has a gate that receives an inverse sleep signal SLPB (not shown) generated by the inverse of the sleep signal SLP.

Please amend paragraph 0080 as follows:

The undershoot preventive circuit 62 includes an N-channel-type MOS (metal oxide semiconductor) transistor 81 (hereinafter referred to as an N-MOS transistor 81), an operations amplifier 83, and a current control circuit 83. The N-MOS transistor 81 operates as a load to consume a current Ia flowing from the output terminal of the smoothing circuit 32 to [the grounding] ground. The operational amplifier 82 operates as a voltage comparator for comparing the divided voltage Vd output from the voltage dividing circuit 74 to the reference voltage Vr1 output from the Vr1 generator 75, and outputs a binary signal in response to the comparison result. The undershoot preventive circuit 62 further includes a current control circuit 83. The current control circuit 83 controls the operation of the N-MOS transistor 81 in accordance with the signal output from the operational amplifier 82 so as to control the current [ia] Ia flowing from the output terminal of the smoothing circuit 32. The operational amplifier 82, the voltage

dividing circuit 74, and the Vr1 generator 75 together form a voltage determination circuit.

Please amend paragraph 0081 as follows:

In the undershoot preventive circuit 62, when the mode is changed from the normal operation mode to the sleep mode, the sleep signal SLP in a high state is output from the CPU 11. Accordingly, the operational amplifier 82 and the current control circuit 83 are caused to stop the respective operations and, at the same time, the gate of the N-MOS transistor 81 is turned off and is out of conduction. Since the P-MOS transistor 41 is in an on state and is [of conduction] conducting, the voltage Vo is held at a level around the power source voltage VDD.

Please amend paragraph 0083 as follows:

When the low signal is input from the operational amplifier 82 to the current control circuit 83, the current control circuit 83 raises a gate voltage Vg of the N-MOS transistor 81. As a result, the N-MOS transistor 81 generate the current [ia] Ia in response to the gate voltage Vg input, as shown in Fig. 9. The voltage Vd is gradually reduced from the level of the power source voltage VDD to the predetermined voltage Va. During this reduction of the voltage Vd, the operational amplifier 82 changes the output from the low voltage to a high level voltage when the divided voltage Vd is reduced to a level smaller than the reference voltage Vr1.

Please amend paragraph 0084 as follows:

When the operational amplifier 82 outputs a high signal to the current control circuit 83, the current control circuit 83 controls the gate voltage Vg of the N-MOS transistor 81 in a way as shown in Fig. 10. That is, the gate voltage Vg is linearly raised during a predetermined time t1 and is continuously raised during a predetermined time t2. Further, the gate voltage Vg is held at a level of the power source voltage VDD during a predetermined time t3 and is reduced from the level of the voltage Vg to [the grounding] ground level during a predetermined time t4. During these operations, the current Ia flowing through the N-MOS transistor 81 is changed in a way as shown in Fig. 9. The current during the predetermined time t3 is a saturated current. Also, during these operations, the voltage level of the gate voltage Vg is changed in a way as shown in Fig. 10. The gate voltage Vg is continuously raised in the predetermined time t2 at the same voltage raising pace as in a predetermined time t1 after the predetermined time t1, as shown in Fig. 10. This is because the duty control circuit 72 takes a certain delay time before starting the control of the operation of the P-MOS transistor 41 after the voltage level of the voltage Vo is changed to the predetermined voltage Va.

Please amend paragraph 0086 as follows:

The current control circuit 83 is previously provided with various kinds of settings associated with the gate voltage of the N-MOS transistor 81 so that the voltage regulator 3 starts its operation and the load current IOU flows from the smoothing circuit 32 through the voltage regulator 3 during the time the current control circuit 83 reduces the gate

voltage of the N-MOS transistor 81 to [the grounding] ground level. More specifically, the above-mentioned various kinds of settings includes the voltage raising pace of the gate voltage Vg of the N-MOS transistor 81, the predetermined times t2 and t3 in which the gate voltage Vg is held at the level of the power source voltage VDD, and the pace of reducing the gate voltage Vg from the level of the power source voltage VDD to the [the grounding] ground level.

Please amend paragraph 0089 as follows:

When the above-described operations are performed, the voltage Vo is changed in a way as shown in Fig. 12. As a result, the voltage Vo can be prevented from the undershooting during the time the mode is changed from the sleep mode to the normal operation mode and from the overshooting during the time the mode is changed from the normal operation mode to the sleep mode. In addition, the overshoot preventive circuit 63 also [has a function for] prevents an excessive current flowing from the P-MOS transistor 41 in the sleep mode when a short circuit occurs in a load connected to the smoothing circuit 32. With this, the power supply apparatus 1 can prevent an excessive current output from the DC-to-DC converter 2 in the sleep mode.

Please amend paragraph 0100 as follows:

This [paten] patent specification is based on Japanese patent applications, No. JPAP2001-038394 filed on February 15, 2001 and No. JPAP2001-189792 filed on June 22, 2001 in the Japanese Patent Office, the entire contents of which are incorporated by reference

herein.

IN THE CLAIMS:

1. (amended) A power supply apparatus, comprising:

a DC-to-DC converter [arranged and configured to perform a voltage conversion] for converting a voltage of a [source] power source supplied from a direct current power source to a first predetermined voltage, said first predetermined voltage being lower than said voltage of said source power; and

a voltage regulator [arranged and configured to carrying out a voltage regulation] for regulating said first predetermined voltage of said source power to at least a second predetermined voltage, said second predetermined voltage being lower than said first predetermined voltage.

2. (amended) [A] The power supply apparatus [as defined in] of Claim 1, wherein said DC-to-DC converter is turned into a non-active state to stop said voltage conversion and [straight] passes said voltage of said [source] power source when an operation mode is changed to a sleep mode.

3. (amended) [A] The power supply apparatus [as defined in] of Claim 2, wherein said DC-to-DC converter comprising:

a switching circuit arranged and configured to perform a switching operation for switching said [source] power source and to output a pulsating current voltage;

a smoothing circuit [arranged and] configured to smooth said pulsating current voltage output by said switching circuit and to output a smoothed voltage to said voltage regulator; and

a controller [arranged and] configured to detect said smoothed voltage output from said smoothing circuit and to control said switching circuit to change a performance of said switching operation in response to a detection result of said smoothed voltage so that said smoothed voltage output by said smoothing circuit is substantially equal to said first predetermined voltage,

wherein said controller is turned into a non-active state to cause said switching circuit to stop said switching operation so as to pass said voltage of said [source] power source through said switching circuit and to output said voltage of said [source] power source to said smoothing circuit when said operation mode is changed to said sleep mode.

4. (amended) [A] The power supply apparatus [as defined in] of Claim 1, wherein said DC-to-DC converter outputs said voltage of said [source] power source without performing said voltage conversion when said operation mode is changed to said sleep mode.

5. (amended) [A] The power supply apparatus [as defined in] of Claim 4, wherein said converter comprising:

a switching circuit [arranged and configured to perform a switching operation] for switching said [source] power source and outputting a pulsating current voltage;

a smoothing circuit [arranged and configured to smooth] for smoothing said pulsating current voltage output from said switching circuit and to output a smoothed voltage to said voltage regulator; and

a controller [arranged and] configured to detect said smoothed voltage output from said smoothing circuit and to control said switching circuit to change [a performance of] said switching operation in response to a detection result of said smoothed voltage so that said

smoothed voltage output from said smoothing circuit is substantially equal to said first predetermined voltage,

wherein said controller causes said switching circuit to stop said switching operation so as to pass said voltage of said [source] power source through said switching circuit and to output said voltage of said [source] power source to said smoothing circuit when said operation mode is changed to said sleep mode.

6. (amended) [A] The power supply apparatus [as defined in] of Claim 5, wherein said controller connects a load to an output terminal of said smoothing circuit and controls a current flowing said load so as to reduce said voltage output from said smoothing circuit to said first predetermined voltage when said voltage output from said smoothing circuit is lower than said first predetermined voltage and when said operation mode is changed to a normal operation mode.

7. (amended) [A] The power supply apparatus [as defined in] of Claim 6, wherein said controller [comprising] comprises:

a transistor which operates as said load;

a comparator [which performs a first comparison] for comparing said voltage output from said smoothing circuit with said first predetermined voltage when said operation mode is changed to said normal operation mode and outputs a first comparison result; and

a current control circuit [arranged and] configured to control said transistor to produce a current flowing therethrough in response to said first comparison result of said comparator when said operation mode is changed to said normal operation mode.

8. (amended) [A] The power supply apparatus [as defined in] of Claim 7, wherein said current control circuit controls said transistor to increase said current at a first predetermined pace when said voltage output from said smoothing circuit is determined as greater than said first predetermined voltage based on said first comparison result performed by said comparator.

9. (amended) [A] The power supply apparatus [as defined in] of Claim 7, wherein said current control circuit controls said transistor to continue to increase said current at said first predetermined pace for a first predetermined time period when said voltage output from said smoothing circuit is determined as substantially equal to said first predetermined voltage based on said first comparison result performed by said comparator, and controls said transistor to produce a saturated current flowing therethrough for a second predetermined time period immediately after said first predetermined time period.

10. (amended) [A] The power supply apparatus [as defined in] of Claim 9, wherein said current control circuit controls said transistor to decrease said current at a second predetermined pace for a third predetermined time period immediately after said second predetermined time period.

11. (amended) [A] The power supply apparatus [as defined in] of Claim 5, wherein said controller detects a current output from said switching circuit and controls said switching circuit to vary said current in response to said detected current when said operation mode is changed to said sleep mode.

12. (amended) [A] The power supply apparatus [as defined in] of Claim 11, wherein said controller controls said switching circuit to straight output said voltage of said [source] power source to said smoothing circuit when said current detected is smaller than a predetermined value and to reduce said current output therefrom to a value smaller than said predetermined value in a predetermined manner when said current is greater than said predetermined value.

13. (amended) [A] The power supply apparatus [as defined in] of Claim 5, wherein said controller performs a second comparison between a reference voltage dropping at a substantially constant pace and said voltage output from said smoothing circuit in response to said detected voltage and, according to a result of said second comparison, controls a duty cycle of said switching operation performed by said switching circuit during a time said voltage output from said smoothing circuit is reduced to said first predetermined voltage, when said operation mode is changed to said normal operation mode.

14. (amended) [A] The power supply apparatus [as defined in] of Claim 13, wherein said controller performs a third comparison between another predetermined reference voltage and said voltage output from said smoothing circuit in response to said detected voltage and, according to a result of said third comparison, controls a duty cycle of said switching operation performed by said switching circuit when said voltage output from said smoothing circuit is reduced to said first predetermined voltage.

15. (amended) A power supply apparatus, comprising:

converting means for performing a DC-to-DC conversion [to achieve a voltage conversion] for converting a voltage of a [source] power source supplied from a direct current power source to a first predetermined voltage, said first predetermined voltage being lower than said voltage of said [source] power source; and

regulating means for carrying out a voltage regulation for regulating said first predetermined voltage of said [source] power source to at least a second predetermined voltage, said second predetermined voltage being lower than said first predetermined voltage.

16. (amended) [A] The power supply apparatus [as defined in] of Claim 15, wherein said converting means is turned into a non-active state to stop said voltage conversion and straight passes said voltage of said [source] power source when an operation mode is changed to a sleep mode.

17. (amended) [A] The power supply apparatus [as defined in] of Claim 16, wherein said DC-to-DC converter comprising:

switching means [for performing a switching operation] for switching said [source] power source and [to output] outputting a pulsating current voltage;

smoothing means for smoothing said pulsating current voltage output by said switching means and to output a smoothed voltage to said regulating means; and

controlling means for detecting said smoothed voltage output from said smoothing means and to control said switching means to change a performance of said switching operation in response to a detection result of said smoothed voltage so that said smoothed voltage output by said smoothing means is substantially equal to said first predetermined voltage,

wherein said controlling means is turned into a non-active state to cause said switching means to stop said switching operation so as to pass said voltage of said [source] power source through said switching means and to output said voltage of said [source] power source to said smoothing means when said operation mode is changed to said sleep mode.

18. (amended) [A] The power supply apparatus [as defined in] of Claim 15, wherein said converting means outputs said voltage of said [source] power source without performing said voltage conversion when said operation mode is changed to said sleep mode.

19. (amended) [A] The power supply apparatus [as defined in] of Claim 18, wherein said converting means comprising:

switching means [for performing a switching operation] for switching said [source] power source and outputting a pulsating current voltage;

smoothing means for smoothing said pulsating current voltage output from said switching means and to output a smoothed voltage to said regulating means; and

controlling means for detecting said smoothed voltage output from said smoothing means and to control said switching means to change a performance of said switching operation in response to a detection result of said smoothed voltage so that said smoothed voltage output from said smoothing means is substantially equal to said first predetermined voltage,

wherein said controlling means causes said switching means to stop said switching operation so as to pass said voltage of said [source] power source through said switching means and to output said voltage of said [source] power source to said smoothing means when said operation mode is changed to said sleep mode.

20. (amended) [A] The power supply apparatus [as defined in] of Claim 19, wherein said controlling means connects a load to an output terminal of said smoothing means and controls a current flowing through said load so as to reduce said voltage output from said smoothing means to said first predetermined voltage when said voltage output from said smoothing means is lower than said first predetermined voltage and when said operation mode is changed to a normal operation mode.

21. (amended) [A] The power supply apparatus [as defined in] of Claim 20, wherein said controlling means comprising:

a transistor which operates as said load;

comparing means for performing a first comparison for comparing said voltage output from said smoothing means with said first predetermined voltage when said operation mode is changed to said normal operation mode and outputs a first comparison result; and

current controlling means controlling said transistor to produce a current flowing therethrough in response to said first comparison result of said comparing means when said operation mode is changed to said normal operation mode.

22. (amended) [A] The power supply apparatus [as defined in] of Claim 21, wherein said current controlling means controls said transistor to increase said current at a first predetermined pace when said voltage output from said smoothing means is determined as greater than said first predetermined voltage based on said first comparison result performed by said comparing means.

23. (amended) [A] The power supply apparatus [as defined in] of Claim 21, wherein said current controlling means controls said transistor to continue to increase said current at said first predetermined pace for a first predetermined time period when said voltage output from said smoothing means is determined as substantially equal to said first predetermined voltage based on said first comparison result performed by said comparing means, and controls said transistor to produce a saturated current flowing therethrough for a second predetermined time period immediately after said first predetermined time period.

24. (amended) [A] The power supply apparatus [as defined in] of Claim 23, wherein said current controlling means controls said transistor to decrease said current at a second predetermined pace for a third predetermined time period immediately after said second predetermined time period.

25. (amended) [A] The power supply apparatus [as defined in] of Claim 19, wherein said controlling means detects a current output from said switching means and controls said switching means to vary said current in response to said detected current when said operation mode is changed to said sleep mode.

26. (amended) [A] The power supply apparatus [as defined in] of Claim 25, wherein said controlling means controls said switching means to straight output said voltage of said [source] power source to said smoothing means when said current detected is smaller than a predetermined value and to reduce said current output therefrom to a value smaller than said predetermined value in a predetermined manner when said current is greater than said predetermined value.

27. (amended) [A] The power supply apparatus [as defined in] of Claim 19, wherein said controlling means performs a second comparison between a reference voltage dropping at a substantially constant pace and said voltage output from said smoothing means in response to said detected voltage and, according to a result of said second comparison, controls a duty cycle of said switching operation performed by said switching means during a time said voltage output from said smoothing means is reduced to said first predetermined voltage, when said operation mode is changed to said normal operation mode.

28. (amended) [A] The power supply apparatus [as defined in] of Claim 27, wherein said controlling means performs a third comparison between another predetermined reference voltage and said voltage output from said smoothing means in response to said detected voltage and, according to a result of said third comparison, controls a duty cycle of said switching operation performed by said switching means when said voltage output from said smoothing means is reduced to said first predetermined voltage.

29. (amended) A method of power supply, comprising the steps of:

using [performing a DC-to-DC conversion with] a DC-to-DC converter to convert [achieve a voltage conversion for converting] a voltage of a [source] power source supplied from a direct current power source to a first predetermined voltage, said first predetermined voltage being lower than said voltage of said [source] power source; and

regulating said first predetermined voltage of said [source] power source to at least a second predetermined voltage, said second predetermined voltage being lower than said first predetermined voltage.

30. (amended) [A] The method [as defined in] of Claim 29, wherein said performing step turns said DC-to-DC converter into a non-active state to stop said DC-to-DC conversion and [straight] passes said voltage of said [source] power source straight through said DC-to-DC converter to said voltage regulator when an operation mode is changed to a sleep mode.

31. (amended) [A] The method [as defined in] of Claim 30, wherein said performing step comprising the steps of:

executing a switching operation for switching said [source] power source to output a pulsating current voltage;

smoothing said pulsating current voltage output by said switching circuit to output a smoothed voltage to said voltage regulator;

detecting said smoothed voltage output in said smoothing step;

changing a performance of said switching operation in response to a detection result of said smoothed voltage so that said smoothed voltage output in said smoothing step is substantially equal to said first predetermined voltage; and

stopping said switching operation when said operation mode is changed to said sleep mode so as to apply said voltage of said [source] power source to said smoothing circuit.

32. (amended) [A] The method [as defined in] of Claim 29, wherein said DC-to-DC converter outputs said voltage of said [source] power source without performing said voltage conversion when said operation mode is changed to said sleep mode.

33. (amended) [A] The method [as defined in] of Claim 32, wherein said performing step comprising the steps of:

executing a switching operation for switching said [source] power source to output a pulsating current voltage;

smoothing said pulsating current voltage output in said switching step to output a smoothed voltage to said voltage regulator;

detecting said smoothed voltage output in said smoothing step;

changing a performance of said switching operation in response to a detection result of said smoothed voltage so that said smoothed voltage output in said smoothing step is substantially equal to said first predetermined voltage; and

stopping said switching operation when said operation mode is changed to said sleep mode so as to apply said voltage of said [source] power source to said smoothing circuit.

34. (amended) [A] The method [as defined in] of Claim 32, further comprising steps of:

providing a transistor as a load;

applying said voltage output in said smoothing step to said transistor so that a current flows through said transistor when said voltage output in said smoothing step is lower than said first predetermined voltage and when said operation mode is changed to a normal operation mode; and

adjusting said current flowing said load so as to reduce said voltage output in said smoothing step to said first predetermined voltage.

35. (amended) [A] The method [as defined in] of Claim 34, wherein said adjusting step comprising the steps of:

performing a first comparison for comparing said voltage output in said smoothing step with said first predetermined voltage when said operation mode is changed to said normal operation mode to output a first comparison result; and

causing said transistor to produce a current flowing therethrough in response to said first comparison result of said comparing step when said operation mode is changed to said normal operation mode.

36. (amended) [A] The method [as defined in] of Claim 35, wherein said causing step causes said transistor to increase said current at a first predetermined pace when said voltage output in said smoothing step is determined as greater than said first predetermined voltage based on said first comparison result performed in said comparing step.

37. (amended) [A] The method [as defined in] of Claim 35, wherein said causing step causes said transistor to continue to increase said current at said first predetermined pace for a first predetermined time period when said voltage output in said smoothing step is determined as substantially equal to said first predetermined voltage based on said first comparison result performed in said comparing step, and causes said transistor to produce a saturated current flowing therethrough for a second predetermined time period immediately after said first predetermined time period.

38. (amended) [A] The method [as defined in] of Claim 37, wherein said causing step causes said transistor to decrease said current at a second predetermined pace for a third predetermined time period immediately after said second predetermined time period.

39. (amended) [A] The method [as defined in] of Claim 33, further comprising the steps of:

detecting a current output in said switching step when said operation mode is changed to said sleep mode; and

instructing said switching step to change said current in response to said detected current.

40. (amended) [A] The method [as defined in] of Claim 39, wherein said instructing step instructs said switching step to straight output said voltage of said [source] power source to said smoothing step when said current detected is smaller than a predetermined value and to reduce said current output in said switching step to a value smaller than said predetermined value in a predetermined manner when said current is greater than said predetermined value.

41. (amended) [A] The method [as defined in] of Claim 33, further comprising the steps of:

performing a second comparison between a reference voltage dropping at a substantially constant pace and said voltage output in said smoothing step in response to said detected voltage during a time said voltage output in said smoothing step is reduced to said first predetermined voltage; and

determining a duty cycle of said switching operation performed in said switching step according to a result of said second comparison.

42. (amended) [A] The method [as defined in] of Claim 41, further comprising the steps of:

performing a third comparison between another predetermined reference voltage and said voltage output in said smoothing circuit in response to said detected voltage; and

controlling said duty cycle of said switching operation performed in said switching step according to a result of said third comparison when said voltage output in said smoothing step is reduced to said first predetermined voltage.